WHAT IS CLAIMED IS:

1. An apparatus comprising:

a first dynamic logic circuit having an output node on which a scan value is provided during scan; and

one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, and wherein an output of the second dynamic logic circuits is sampled in response to the scan value during scan.

2. The apparatus as recited in claim 1 further comprising:

a first clock buffer circuit configured to generate a first clock controlling at least evaluation of the second dynamic logic circuits, wherein the first clock buffer circuit is configured to generate at least one evaluate pulse on the first clock prior to sampling the output of the second dynamic logic circuits, the output responsive to the scan value on the output node of the first dynamic logic circuit; and

circuitry configured to generate a second clock controlling precharge of the first dynamic logic circuit and a third clock controlling evaluation of the first dynamic logic circuit, the circuitry coupled to receive a scan mode signal indicative of whether or not scan is active, wherein the circuitry is configured to isolate the output node of the first dynamic logic circuit from inputs to the first dynamic logic circuit using the second clock and the third clock responsive to the scan mode signal indicating that scan is

active.

3. The apparatus as recited in claim 2 wherein the first clock further controls precharge of the second dynamic logic circuits.

4. The apparatus as recited in claim 2 further comprising a clocked storage device configured to sample the output of the second dynamic logic circuits, wherein the clocked storage device is clocked by a fourth clock.

5. The apparatus as recited in claim 2 wherein the circuitry comprises a second clock buffer circuit configured to generate the second clock and a third clock buffer circuit configured to generate the third clock.

6. The apparatus as recited in claim 5 wherein the third clock buffer circuit comprises:

a series connection of transistors coupled between a first node and ground, the series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and the second transistor has a second control node;

a logic circuit coupled to the second control node and coupled to receive the first signal and the scan mode signal, the logic circuit configured to deactivate the second transistor responsive to the scan mode signal indicating that scan is active.

7. The apparatus as recited in claim 6 wherein the logic circuit is further configured to control the second transistor responsive to the first signal if the scan mode signal

indicates that scan is inactive.

8. The apparatus as recited in claim 5 wherein the second clock buffer circuit comprises:

a series connection of transistors coupled between a first node and ground, the series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and the second transistor has a second control node controlled by an inverse of the first signal, the functional clock operating during functional operation;

a third transistor coupled to the first node, the third transistor having a third control node coupled to receive the scan mode signal.

9. The apparatus as recited in claim 8 further comprising a logic circuit coupled to receive the functional clock and the scan mode signal, wherein the logic circuit is configured to generate the first signal.

10. The apparatus as recited in claim 8 wherein the first signal is further coupled to a fourth control node of a fourth transistor coupled between a power supply and the first node.

11. A clock buffer circuit comprising:

a series connection of transistors coupled between a first node and ground, the series connection of transistors including at least a first transistor and a second transistor, wherein the first transistor has a first control node coupled to receive a first signal corresponding to a functional clock and

the second transistor has a second control node;

a logic circuit coupled to the second control node and coupled to receive the first signal and a first input; and

a third transistor coupled to the first node and having a third control node coupled to receive a second input.

12. The clock buffer circuit as recited in claim 11 wherein the first input and the second input are coupled to ground.

13. The clock buffer circuit as recited in claim 11 wherein the first input is coupled to ground and the second input is coupled to a scan mode signal indicative of whether or not scan is active.

14. The clock buffer circuit as recited in claim 11 wherein the first input is coupled to a scan mode signal indicative of whether or not scan is active and the second input is coupled to ground.

15. The clock buffer circuit as recited in claim 11 wherein the series connection of transistors further comprises a fourth transistor having a fourth control node coupled to receive a condition signal.

16. The clock buffer circuit as recited in claim 11 further comprising a second logic circuit coupled to receive the functional clock and the second input, wherein the second logic circuit is configured to generate the first signal.

17. The clock buffer circuit as recited in claim 11 wherein the first signal is further

coupled to a fourth control node of a fourth transistor coupled between a power supply and the first node.

18. In an apparatus including a first dynamic logic circuit having an output node on which a scan value is provided during scan and one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, the method comprising:

generating at least one evaluate pulse on a first clock controlling at least evaluation of the second dynamic logic circuits;

isolating the output node of the first dynamic logic circuit from inputs to the first dynamic logic circuit using the second clock and the third clock responsive to a scan mode signal indicating that scan is active, the second clock controlling precharge of the first dynamic logic circuit and the third clock controlling evaluation of the first dynamic logic circuit; and

sampling the output of the second dynamic logic circuits subsequent to generating the at least one evaluate pulse, the output responsive to the scan value on the output node of the first dynamic logic circuit.

19. The method as recited in claim 18 further comprising controlling precharge of the second dynamic circuits using the first clock.

20. A computer accessible medium comprising one or more data structures representing:

a first dynamic logic circuit having an output node on which a scan value is provided during scan; and

one or more second dynamic logic circuits, wherein one of the second dynamic logic circuits has an input coupled to the output node of the first dynamic logic circuit, and wherein an output of the second dynamic logic circuits is sampled in response to the scan value during scan.